

FIG. 1

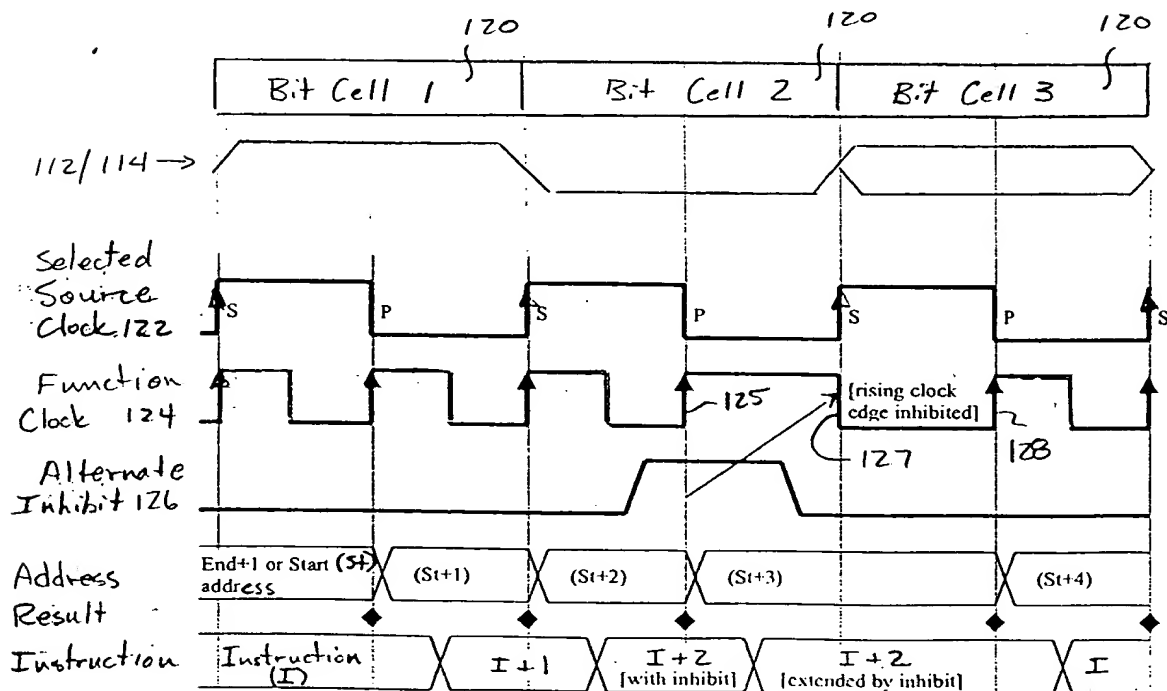
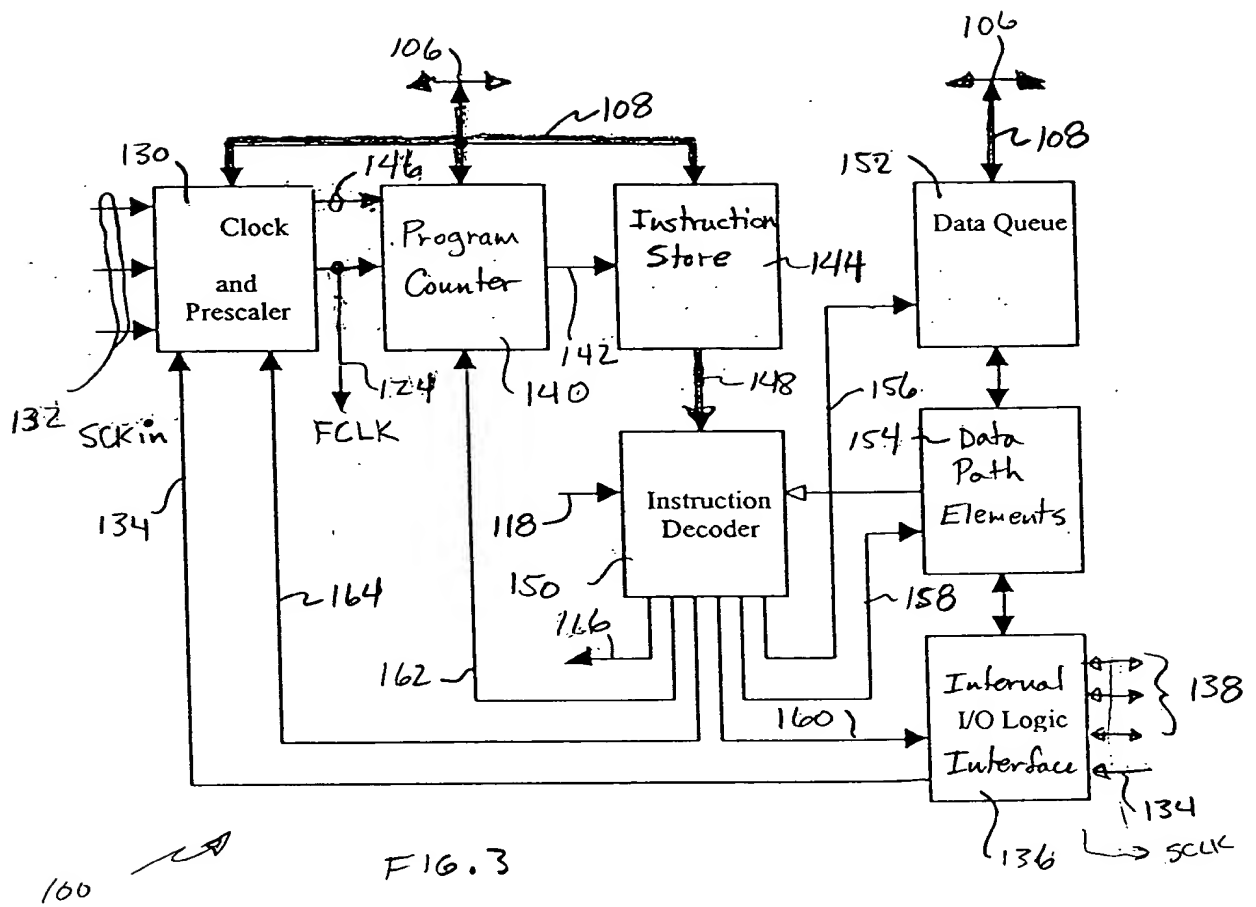


FIG. 2



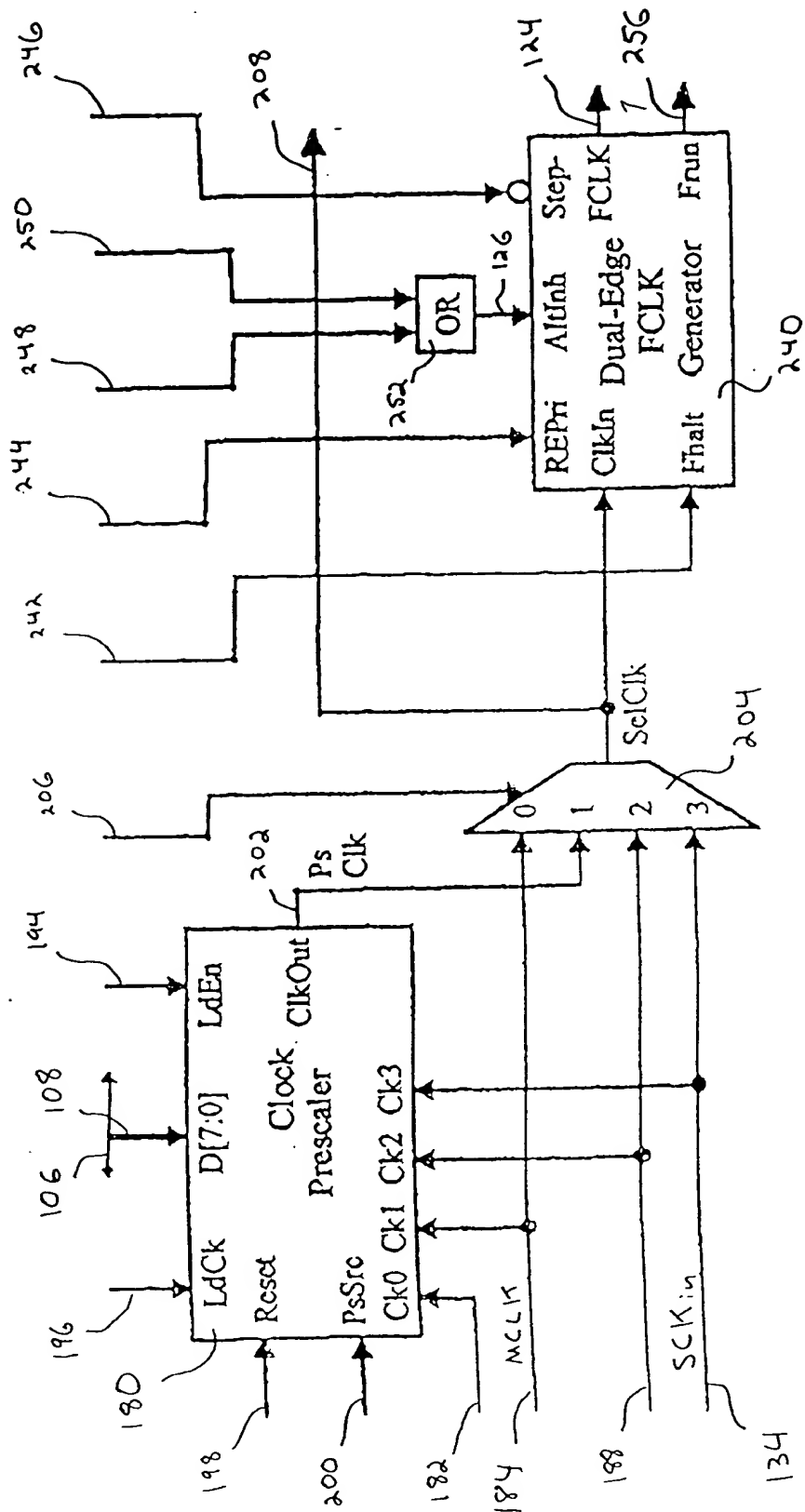
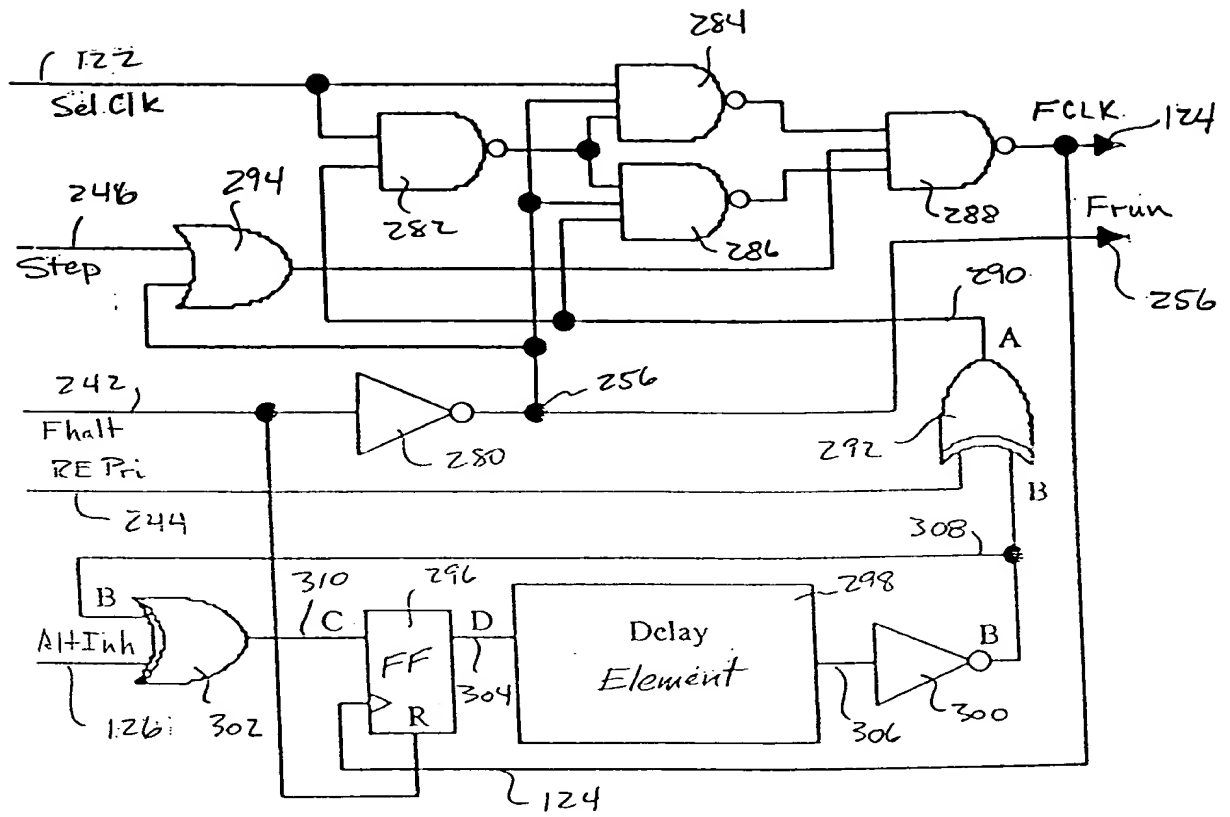


FIG. 4

09717495 "112000



240 ↗ FIG. 5

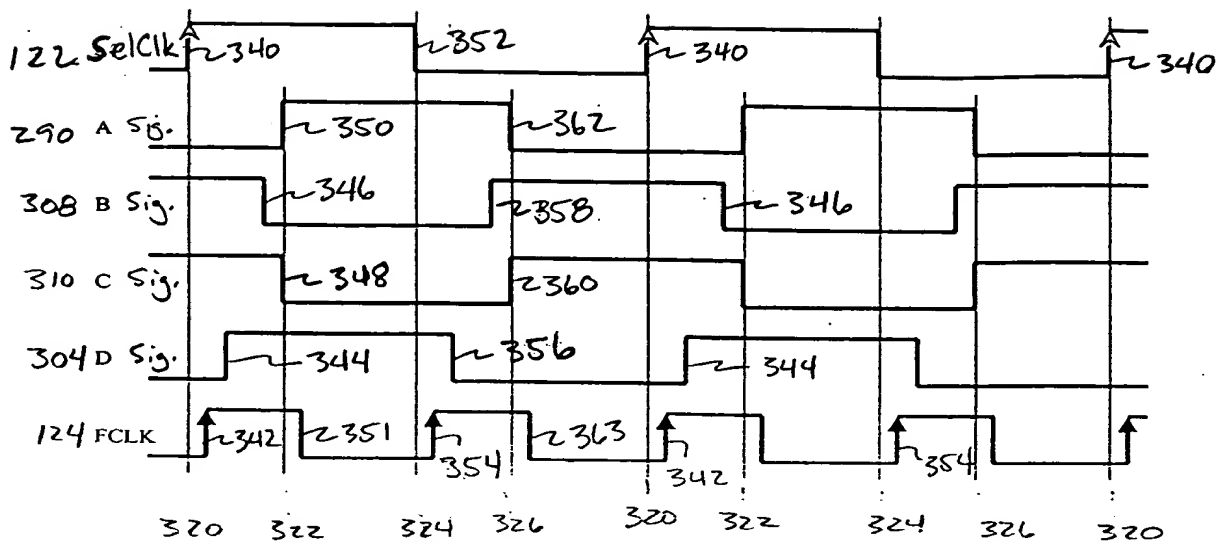


FIG. 6

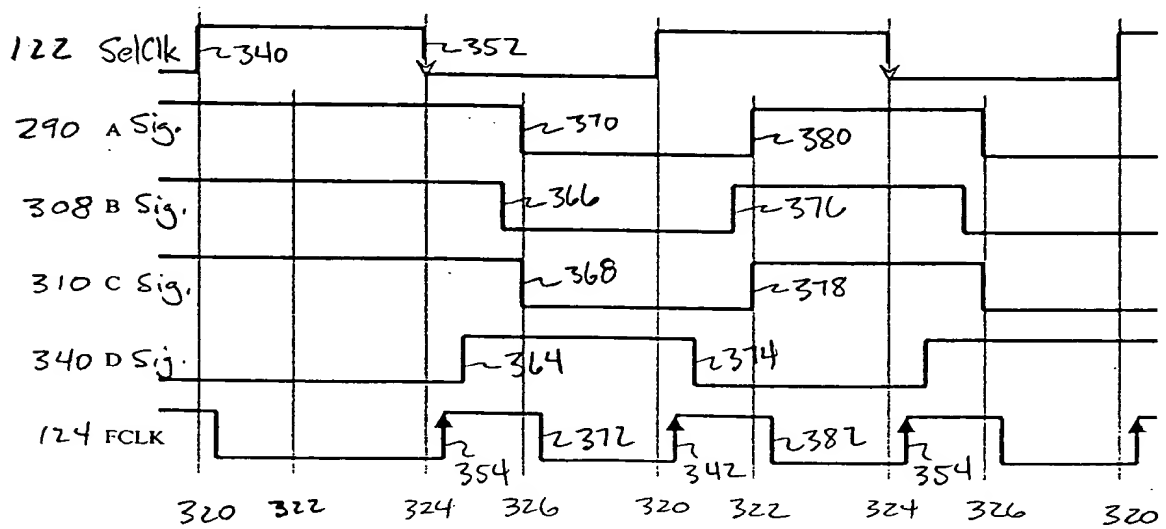


FIG. 7

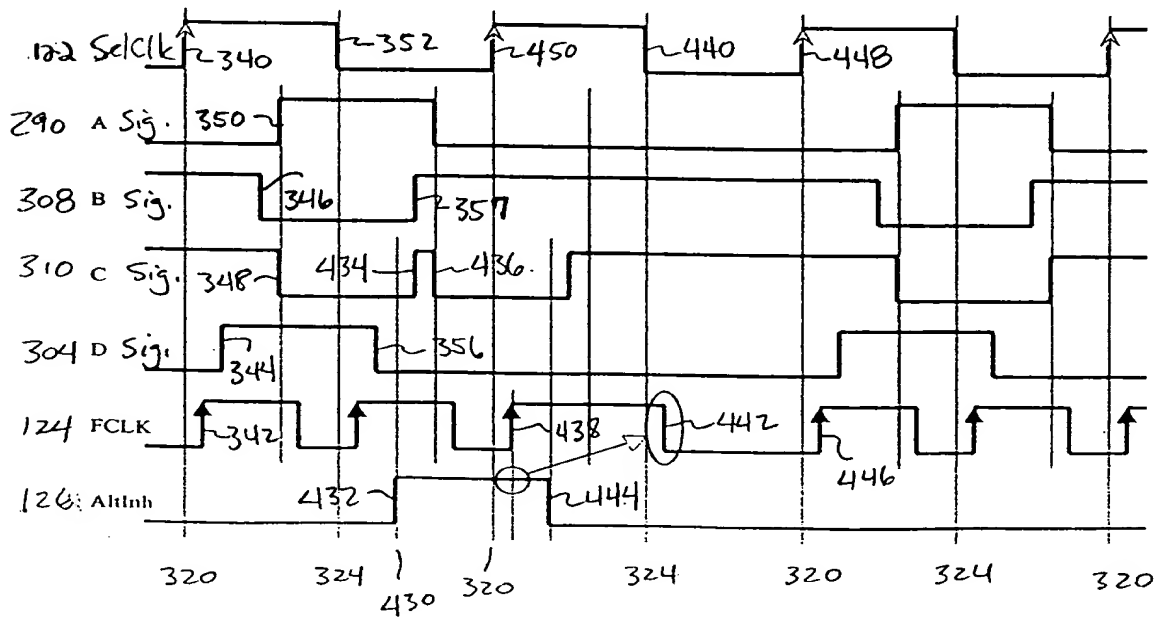
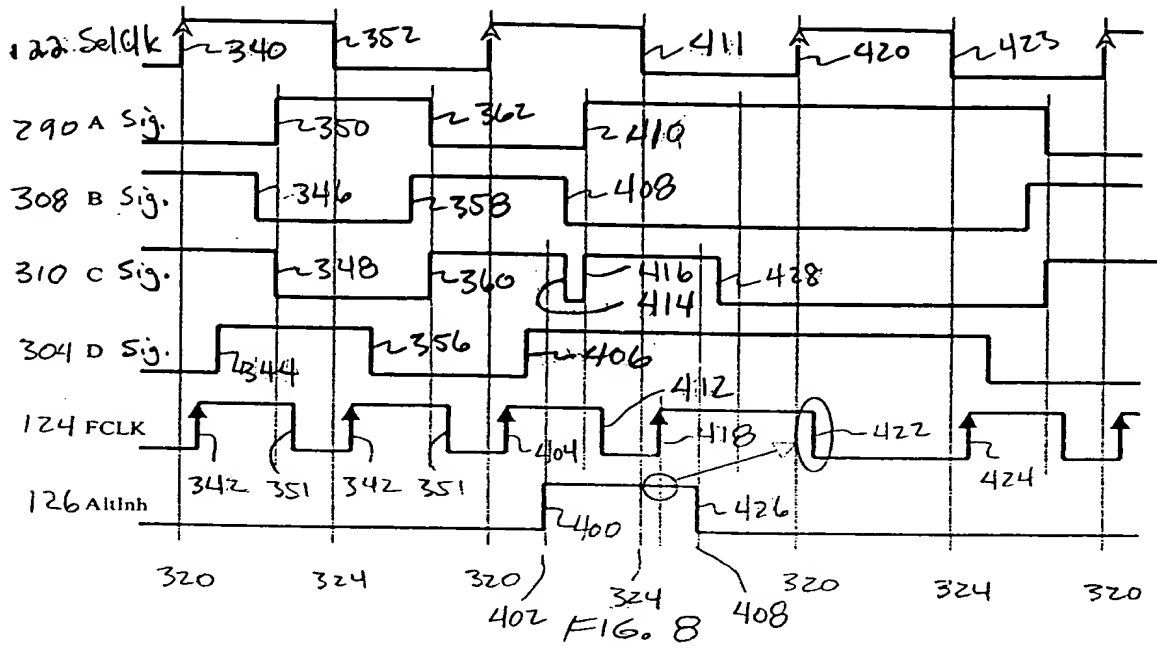
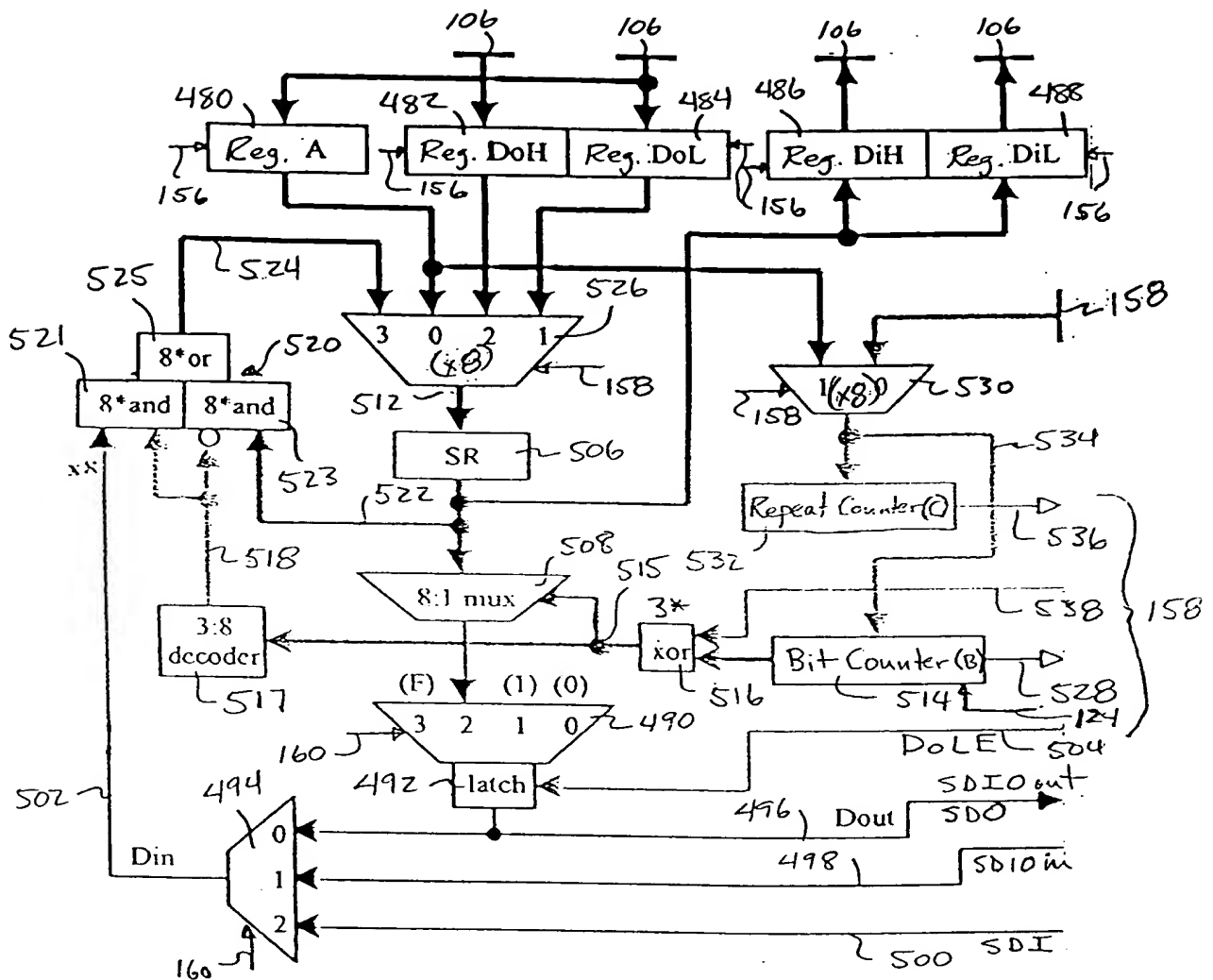


FIG. 9

0971495 - 112000



152/154/136 FIG. 10

552								
Instruction	7	6	5	4	3	2	1	0
Delay / Nop	0	0	0	0	0	0	Count (C)	
							0	Nop
							1	Delay 1, skip alt
							2	Delay 2 (uses C)
							3	Delay 3 (uses C)

550  FIG. 11

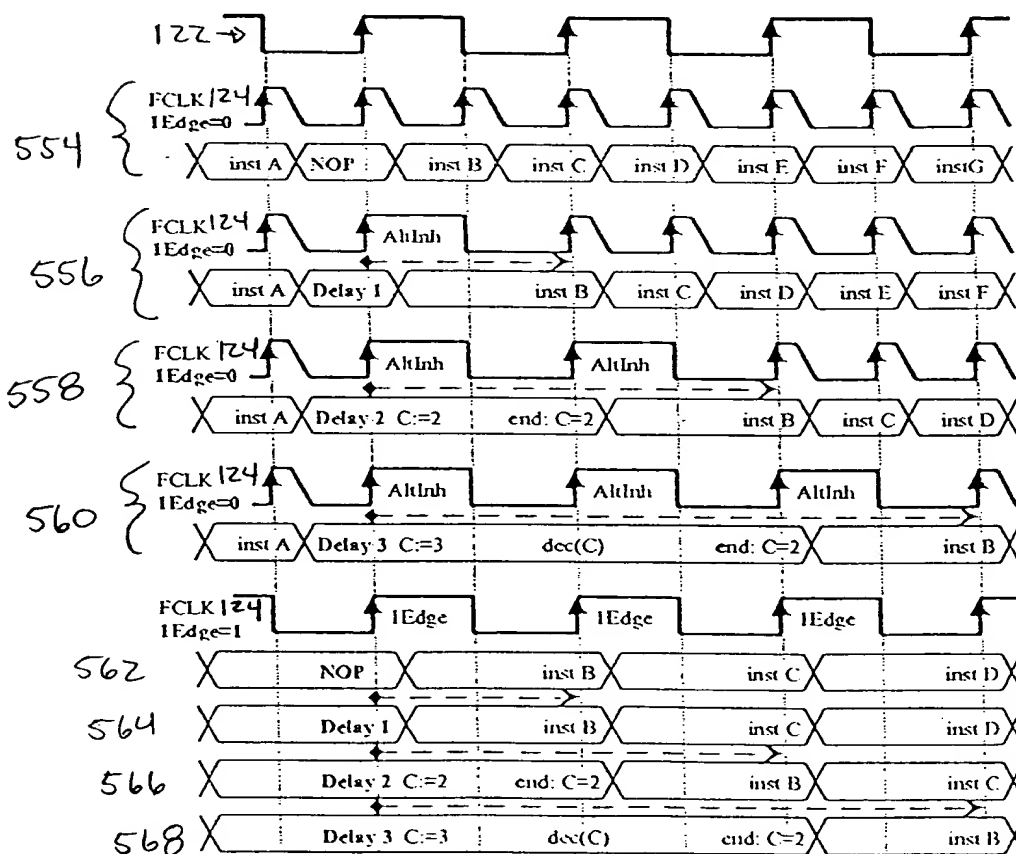


FIG. 12

		592				594		
Instruction	7	6	5	4	3	2	1	0
Wait	0	0	0	1	0	0	Event	

590  FIG. 13

		602				604		
Instruction	7	6	5	4	3	2	1	0
OUTnxb	0	0	1	1	0 (Out)	Count (C)		
INbnx	0	0	1	1	1 (In)	Count (C)		
						0	reserved ^a	
						1	Out/In, skip alt	
						2	Out/In 2 cycles, skip alt	
						3	Out/In 3 cycles, skip alt	
						4	Out/In 4 cycles, skip alt	
						5	Out/In 5 cycles, skip alt	
						6	Out/In 6 cycles, skip alt	
						7	Out/In 7 cycles, skip alt	


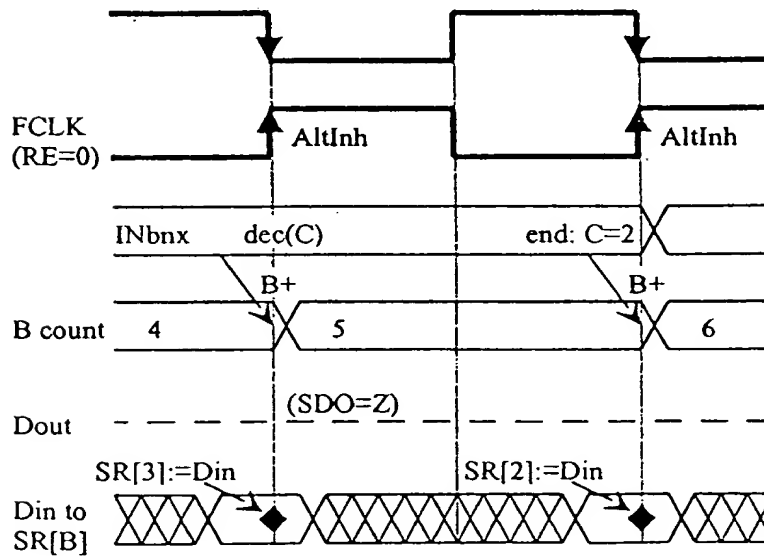
600 

FIG. 14



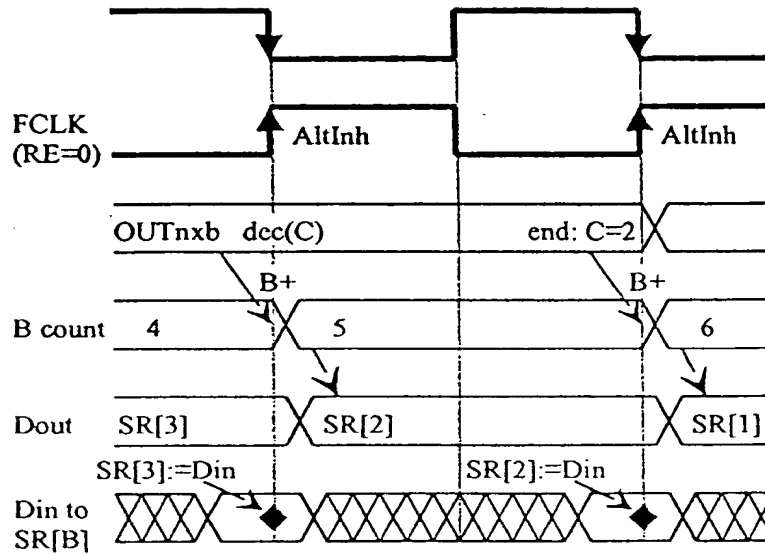


FIG. 17

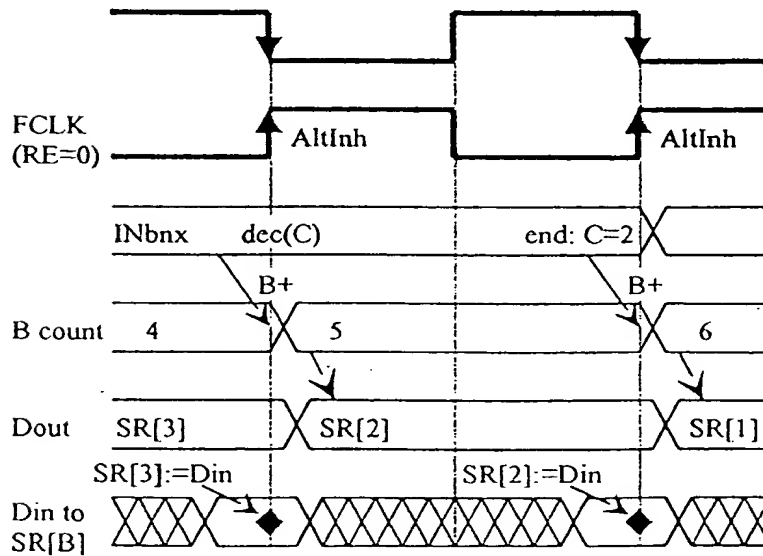


FIG. 18

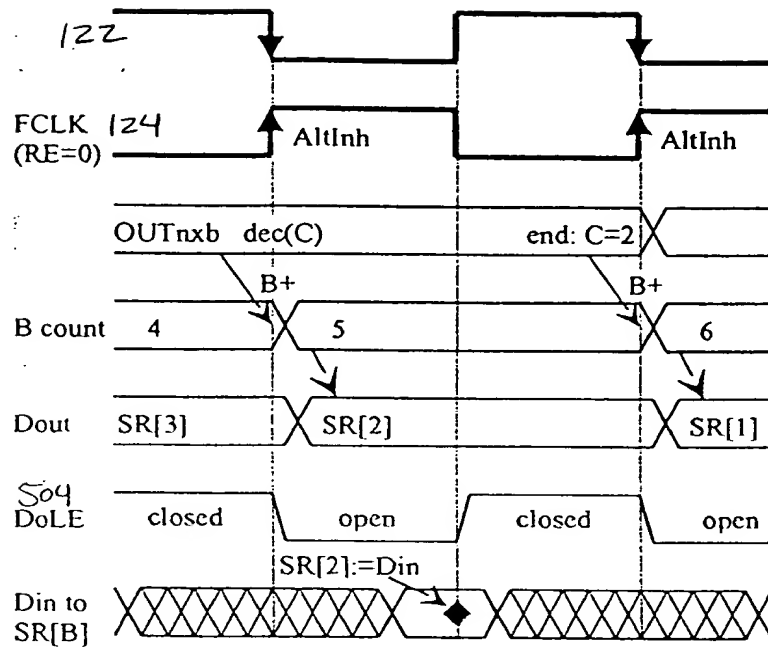


FIG. 19

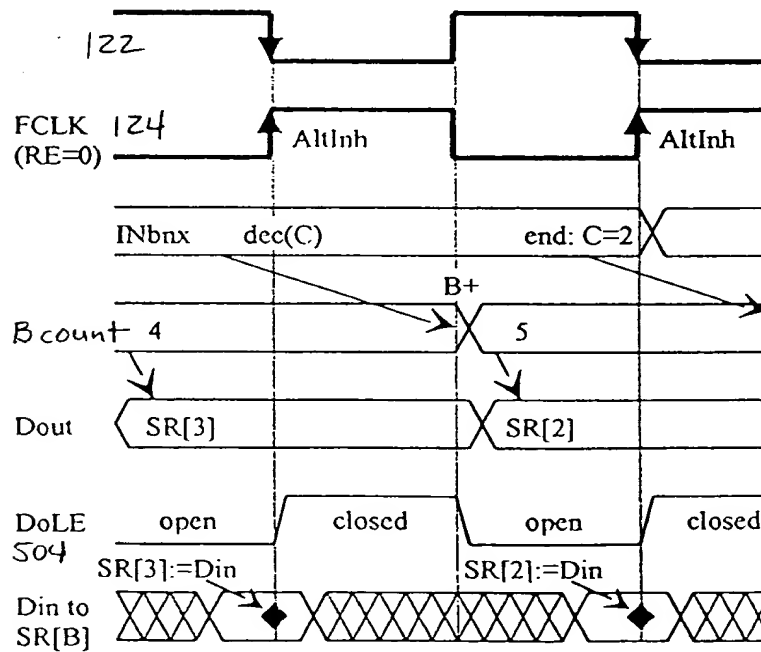


FIG. 20

000217" 56h2T260

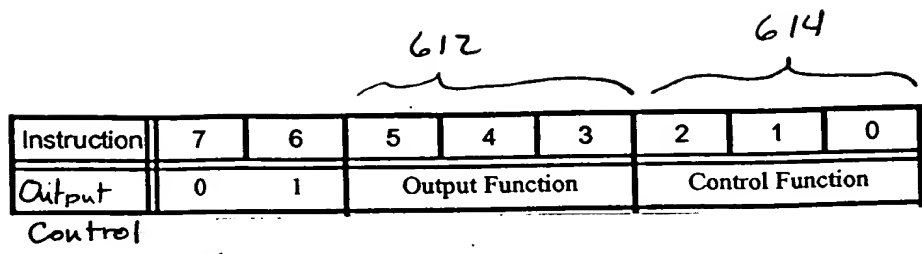


FIG. 21

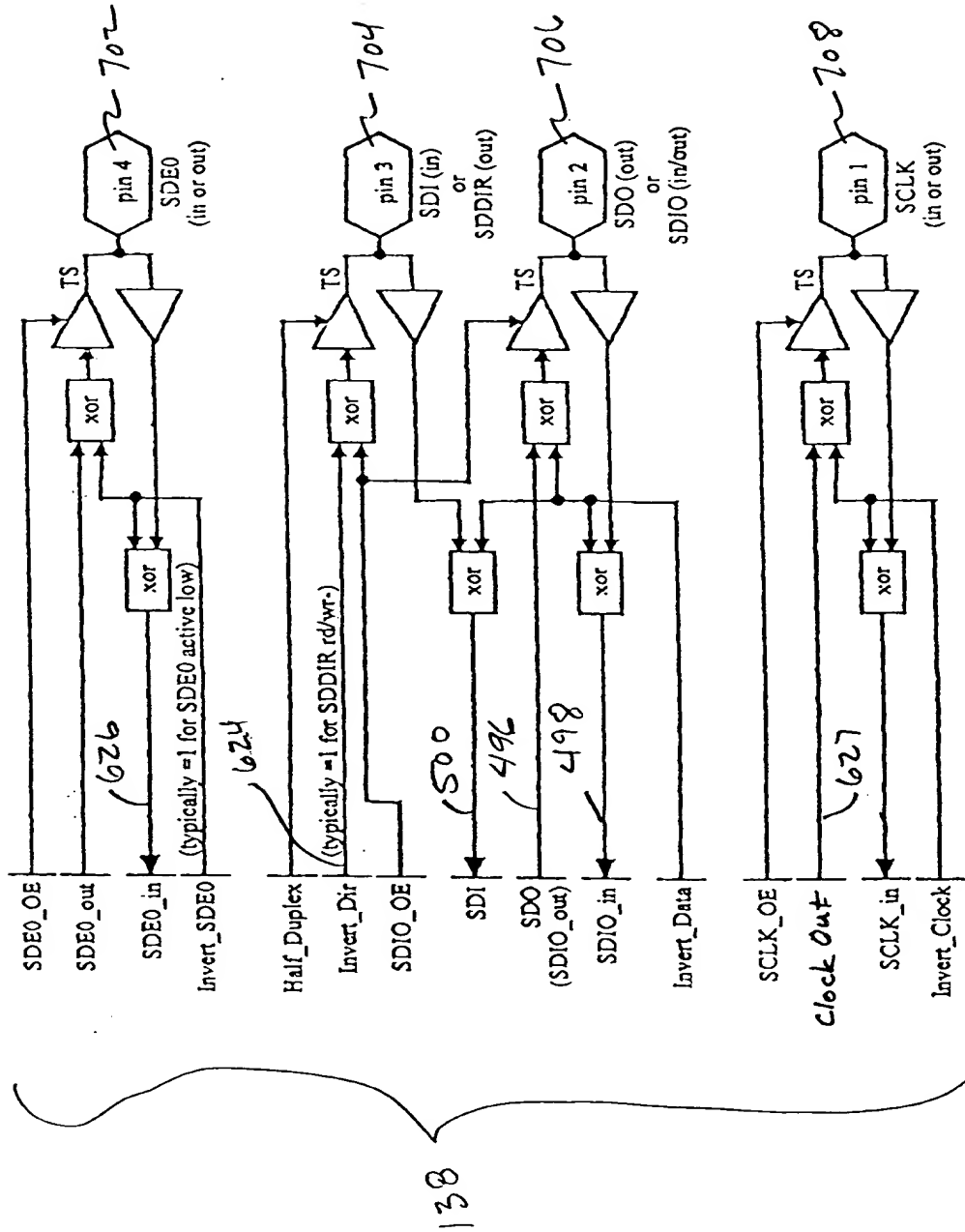


FIG. 22

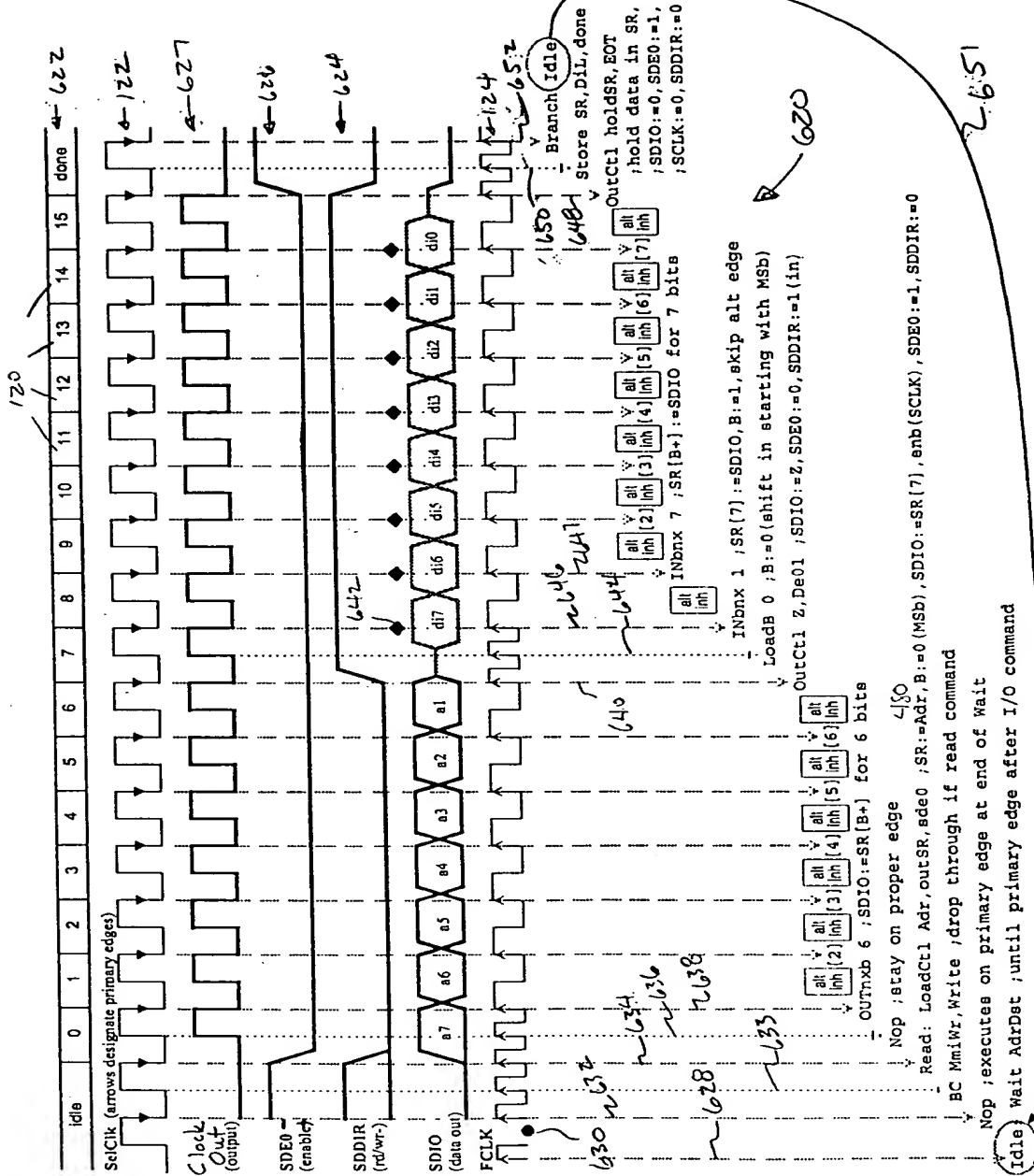


FIG. 23

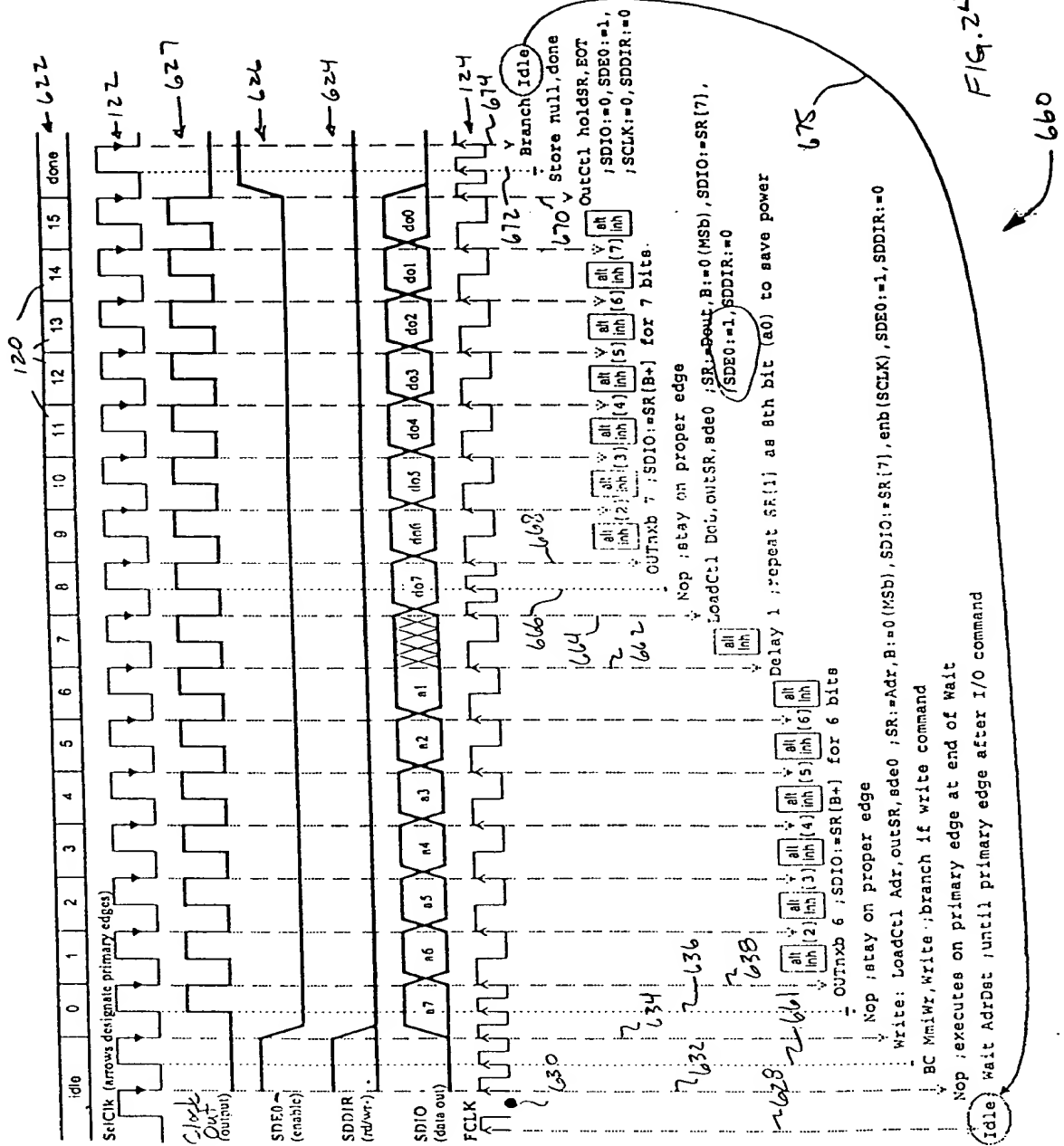


FIG. 24